

Listing of claims:

1-6. (Cancelled).

7. (Previously Presented) A display comprising:

- a chamber to store liquid crystal material,
- a plurality of display transistors arranged in an array across a planar surface of the chamber, the display transistors to define pixels of the display,
- a memory system having a plurality of polymer memory cells provided within the chamber to store liquid crystal, each memory cell being electrically readable and writable.

8. (Original) The display of claim 7, wherein the chamber includes viewable and non-viewable regions and the memory cells are co-located with a non-viewable region thereof.

9. (Original) The display of claim 7, wherein polymer memory cells are co-located with the display transistors.

10. (Previously Presented) The display of claim 7, wherein the memory system comprises:

- the plurality of polymer memory cells,
- a driving line coupled to each of the memory cells, and
- a plurality of data lines, one coupled to each of the memory cells.

11. (Previously Presented) The display of claim 7, wherein the memory system comprises a plurality of layers, each layer comprising:

- memory cells of the plurality of polymer memory cells,
- a driving line coupled to each of the memory cells in the respective layer, and
- a plurality of data lines, one coupled to each of the memory cells in the respective layer.

12. (Original) The display of claim 7, further comprising a backlight coupled to one surface of the display.

13. (Original) The display of claim 7, further comprising a reflector coupled to one surface of the display.

14. (Previously Presented) The display of claim 7, further comprising:

liquid crystal material provided within the chamber,

a first control line on a first surface of the chamber coupled to a display transistor of the plurality of display transistors, and

a second control line provided on a second surface of the chamber opposite the first surface.

15-20. (Cancelled).

21. (Withdrawn) The display of claim 7 arranged in a computer system including a processor, wherein the plurality of display transistors, the memory system, and the processor are electrically coupled together via a communication fabric.

22. (Withdrawn) The display of claim 10 arranged in a computer system including a processor, wherein the plurality of display transistors, the memory system, and the processor are electrically coupled together via a communication fabric.

23. (Withdrawn) The display of claim 11 arranged in a computer system including a processor, wherein the plurality of display transistors, the memory system, and the processor are electrically coupled together via a communication fabric.

24. (Previously Presented) The display of claim 14, wherein the memory system further comprises:

the plurality of polymer memory cells,

a driving line coupled to each of the memory cells, and

a plurality of data lines, one coupled to each of the memory cells,

the driving line and the plurality of data lines being electrically insulated from the first and second control lines.

25. (Previously Presented) The display of claim 14, wherein the memory system comprises a plurality of layers, each layer comprising:

- memory cells of the plurality of polymer memory cells,
- a driving line coupled to each of the memory cells in the respective layer, and
- a plurality of data lines, one coupled to each of the memory cells in the respective layer

the driving line and the plurality of data lines being electrically insulated from the first and second control lines.